EXAR

Interfacing the Microprocessor Serial Interface of the XRT730X/XRT75L0X Family of DS3/E3/STS-1 LIU Devices to the SPI Port of the MC68360 QUICC Device

Interfacing the Microprocessor Serial Interface of the XRT730X/XRT750X Family of DS3/E3/STS-1 LIU Devices to the SPI Port of the MC68360 QUICC Device

1.0 INTRODUCTION

The purpose of this report is to document how one can interface any of the following Exar DS3/E3/STS-1 LIU Devices to the SPI (Serial Peripheral Interface) port of the MC68360 QUICC device.

- XRT7300 – Single Channel DS3/E3/STS-1 LIU IC (5V)
- XRT73L00A – Single Channel DS3/E3/STS-1 LIU IC (3.3V)
- XRT73L02M – 2 Channel DS3/E3/STS-1 LIU IC (3.3V)
- XRT73L03A – 3 Channel DS3/E3/STS-1 LIU IC (3.3V)
- XRT73L03B – 3 Channel (3.3V) DS3/E3/STS-1 LIU IC
- XRT73L04A – 4 Channel (3.3V) DS3/E3/STS-1 LIU IC
- XRT73L04B – 4 Channel (3.3V) DS3/E3/STS-1 LIU IC
- XRT71D00 – DS3/E3/STS-1 Jitter Attenuator IC
- XRT71D03 – 3-Channel DS3/E3/STS-1 Jitter Attenuator IC
- XRT71D04 – 4-Channel DS3/E3/STS-1 Jitter Attenuator IC
- XRT75L00 – Single-Channel DS3/E3/STS-1 LIU w/ Jitter Attenuator IC
- XRT75VL00 – Single-Channel DS3/E3/STS-1 LIU w/ Jitter Attenuator IC
- XRT75L02 – 2-Channel DS3/E3/STS-1 LIU w/ Jitter Attenuator IC
- XRT75L03 – 3-Channel DS3/E3/STS-1 LIU w/ Jitter Attenuator IC
- XRT75R03 – 3-Channel DS3/E3/STS-1 LIU w/ Jitter Attenuator IC, and R3 Capability
- XRT75L04 – 4-Channel DS3/E3/STS-1 LIU w/ Jitter Attenuator IC, and R3 Capability

Basic Approach

The basic approach that one should employ in trying to interface the XRT730X/XRT75L0X device to the MC68360 SPI port is presented in Figure 1.

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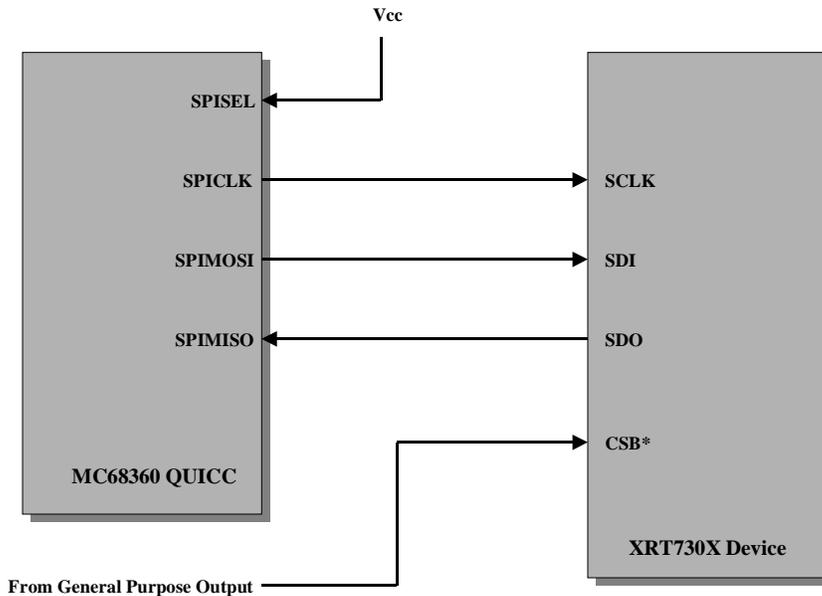
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Figure 1, Simple Illustration on how to interface the XRT730X/XRT75L0X device to the MC68360 SPI Port.

Important Notes:

1. The maximum baud rate that the XRT730X's serial port will support is 2Mbps. However, the maximum baud rate that the XRT75L0X's serial port will support is 20Mbps.

2. The XRT730X/XRT75L0X devices only supports "half-duplex" operation (e.g., data does not flow into the SDI input pin and out of the SDO output pin, at the same time).

3. One must assert the CSB* input, at least 50ns prior to the rising edge of the SPICLK signal.

4. The SDO output of the XRT730X/XRT75L0X device will be tri-stated, when no data is being transmitted. Hence, one should connect a large value resistor (around 100kΩ), from the SDO output to GND. The purpose of doing this is to ensure that the SDO output will be pulled to GND, during idle periods.

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5. Figure 1 assumes that the SPI port, of the MC68360 QUICC device is configured to operate in the Master Mode.

Suggested Settings for the SPI Mode Register (SPMODE), within the MC68360 device. The following table lists the appropriate settings that one should use to properly operate the MC68360 QUICC device, while interfaced to the XRT730X/XRT75L0X devices.

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Table 1, Suggested Settings for the SPMODE register

Bit Number	Name	Setting	Comments
15	----	0	
14	LOOP	0	Normal Operation
13	CI (Clock Invert)	0	The inactive state of SPICLK is "low".
12	CP (Clock Phase)	0	SPICLK begins toggling at the middle of the data transfer.
11	DIV16		User's Choice. Just as long as the SPICLK is not greater than 2MHz.
10	REV	0	XR-T8000 device processes the LSB first.
9	M/S*	1	MC68360 device is a Master
8	EN	1	SPI is enabled.
7, 6, 5, 4	LEN[3:0]	1111	Program for 16 bits/character
3, 2, 1, 0	PM[3:0]		User's Choice